REMARKS

The Office Action dated June 18, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Currently, claims 7-9, 12 and 13 have been allowed. By this Amendment, claim 1 has been further amended to more particularly point out and distinctly claim the invention. Claim 3 has also been amended and is now in independent form. No new matter has been added or amendments made that narrow the scope of any elements of any claims. Accordingly, claims 1-13 are pending in this application and are submitted for consideration.

Applicant acknowledges and thanks the Examiner for indicating that claims 2-6, 10 and 11 would be allowable over the prior art if amended to be in independent form. By this Amendment, claim 3 has been rewritten to be in independent form. Claims 4-6, 10 and 11 depend either directly or indirectly from claim 3. Therefore, it is respectfully submitted that claims 3-6, 10 and 11 are in condition for allowance.

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Sawada (U.S. Patent No. 5,365,481). In making this rejection, the Office Action took the position that Sawada discloses all the elements of the claimed invention. However, Applicant respectfully submits that amended claim 1 recites subject matter that is neither disclosed nor suggested in Sawada.

Applicant's amended claim 1 recites a semiconductor integrated circuit including a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and for inactivating the reset signal after a

predetermined period following the initial supply to terminate an initialization of the internal circuit. A timing changing circuit adjusts the predetermined period in accordance with an internal signal generated by the timing changing circuit at the time of the initial supply.

The Office Action took the position that Sawada discloses the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest such structure and, therefore, fails to provide the advantages that are provided by the present invention. For example, the timing changing circuit of the present invention adjusts a predetermined period in accordance with an internal signal generated by the timing changing circuit, after which, the reset signal is inactivated.

As a result of this claimed configuration, the present invention prevents the reset signal from inactivating before the initialization of the internal circuit terminates and allows reliable initialization of the internal circuit. Additionally, the present invention enables adjustment of the time that the reset signal is inactivated without directly measuring the timing of the reset signal by utilizing the voltage generator transistor.

Sawada discloses a DRAM including a power-on reset circuit 17. Power-on reset circuit 17 receives power supply voltage V_{cc} and generates a first power-on reset signal POR1 which goes "H" during a predetermined period. A power-on reset circuit 18 generates a second power-on reset signal POR2 which goes "H" during a variable period. Power-on reset circuit 19 receives POR1 and POR2 and generates a power-on reset signal for forcibly maintaining predetermined circuit units in the DRAM reset state.

In Sawada, it appears that the internal signal always depends on the signal /RAS when being generated, and is never generated by the circuit 18 itself in the interior

thereof at the time of power-on (the initial supply). In addition, the circuit 18 cannot generate the signal POR2 even if it receives the signal /RAS at the time of the initial supply. This is because the power supply voltage VCC in Sawada is not at a sufficient level at the time of the initial supply.

The Office Action took the position that the input signal to the element 18d in Sawada corresponds to the internal signal of the claimed invention. Moreover, the Office Action stated that the signal TESTX in the present invention corresponds to the signal /RAS in Sawada.

However, Applicant respectfully disagrees, for example, in the present invention, the internal signal can be the adjusting signal RS0 or RS1 and the path of the internal signal does not include the transmission path of the signal TESTX. The internal signal is generated, for example, in the timing changing circuit 24 or 26 without receiving any external signals at the time of the initial supply, irrespective of the signal TESTX supplied from the exterior.

Therefore, Sawada fails to disclose or suggest a timing changing circuit for adjusting the predetermined period in accordance with an internal signal generated by the timing changing circuit at the time of the initial supply of a power supply, and inactivating the reset signal after the predetermined period, as recited in claim 1.

Thus, it is respectfully submitted that the Applicant's invention, as set forth in claim 1, is not anticipated within the meaning of 35 U.S.C. § 102.

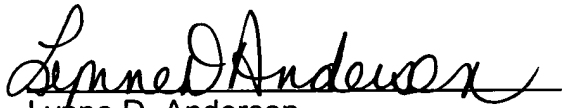
As claim 2 depends from claim 1, Applicant respectfully submits that claim 2 incorporates the patentable aspects thereof and is therefore allowable for at least the same reasons as discussed above.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-6, 10 and 11, (claims 7-9, 12 and 13 already being allowed) and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00042.**

Respectfully submitted,
ARENT FOX KINTNER PLOTKIN & KAHN PLLC



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